AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for increasing the deposition rate of an atomic layer deposition method comprising:

a) positioning a substrate within an atomic layer deposition chamber;

b) flowing a first reactant gas into the atomic layer deposition chamber such that the first reactant gas is adsorbed onto the substrate;

c) flowing an inert gas into the atomic layer deposition chamber to substantially purge the interior of the chamber and leave remaining a residual portion of the first reactant gas; and

d) flowing a second reactant gas into the atomic layer deposition chamber, where the second reactant gas reacts with both the first reactant gas adsorbed onto the substrate and the residual portion of the first reactant gas, thus forming a reacted material layer upon the substrate.

2. (Original) The method of claim 1 further comprising, after step d, flowing an inert gas into the atomic layer deposition chamber to substantially purge the interior of the reactor chamber except for a residual portion of the second reactant gas.

3. (Original) An atomic layer deposition apparatus comprising:

a) an atomic layer deposition chamber;

b) means for positioning a substrate within the atomic layer deposition apparatus;

c) means for flowing a first reactant gas into the atomic layer deposition chamber such that the first reactant gas is adsorbed onto the substrate;

d) means for flowing an inert gas into the atomic layer deposition chamber to substantially purge the interior of the chamber and leave remaining a residual portion of the first reactant gas; and

e) means for flowing a second reactant gas into the atomic layer deposition chamber, where the second reactant gas reacts with both the first reactant gas adsorbed onto the substrate and the residual portion of the first reactant gas, thus forming a reacted material layer upon the substrate.

4. (Original) The apparatus of claim 3 further comprising, means for flowing an inert gas into the atomic layer deposition chamber to substantially purge the interior of the reactor chamber except for a residual portion of the second reactant gas.

5. (Original) A method for forming a microelectronic layer comprising:

providing a substrate;

forming over the substrate a microelectronic layer while employing a deposition method which employs a separately pulsed introduction of a minimum of two reactant materials introduced into a reactor chamber maintained at a pressure of greater than about 500 mtorr.

6. (Original) The method of claim 5 wherein the substrate is employed within a microelectronic product selected from the group consisting of integrated circuit products, ceramic substrate products and optoelectronic products.

7. (Original) The method of claim 5 wherein the deposition method employs a first pulsed reactant gas, a second pulsed reactant gas and a pulsed purge gas.

8. (Original) The method of claim 5 wherein the deposition method employs a first pulsed reactant gas, a second pulsed reactant gas and a non-pulsed purge gas.

9. (Original) The method of claim 5 wherein the minimum of two reactant materials are separately pulsed without overlapping.

10. (Original) The method of claim 5 wherein the minimum of two reactant materials are separately pulsed with overlapping.

11. (Original) The method of claim 5 wherein the microelectronic layer is selected from the group consisting of conductor layers, semiconductor layers and dielectric layers.

12. (Original) The method of claim 5 wherein the microelectronic layer is a conductor barrier layer.

13. (Original) The method of claim 12 wherein the conductor barrier layer is selected from the group consisting of nitrides of titanium, tantalum, tungsten, zirconium, hafnium, molybdenum and niobium.

14. (Original) The method of claim 12 wherein the conductor barrier layer is employed as a capacitor plate layer within a microelectronic capacitor.

15. (Original) A method for forming a microelectronic layer comprising:

providing a substrate;

forming over the substrate a microelectronic layer while employing a deposition method which employs a separately pulsed introduction of a minimum of two reactant materials introduced into a reactor chamber and separated by a reactor chamber purge, where the reactor chamber is maintained at a pressure of greater than about 500 mtorr.

16. (Original) The method of claim 15 wherein the deposition method employs a first pulsed reactant gas, a second pulsed reactant gas and a pulsed purge gas.

17. (Original) The method of claim 15 wherein the deposition method employs a first pulsed reactant gas, a second pulsed reactant gas and a non-pulsed purge gas.

18. (Original) The method of claim 15 wherein the microelectronic layer is selected from the group consisting of conductor layers, semiconductor layers and dielectric layers.

19. (Original) The method of claim 15 wherein the microelectronic layer is a conductor barrier layer.

20. (Original) A method for forming a microelectronic layer comprising:

providing a substrate;

forming over the substrate a microelectronic layer while employing a deposition method which employs a separately pulsed introduction of a minimum of two reactant materials introduced into a reactor chamber, where the reactor chamber is maintained at a pressure of greater than about 500 mtorr such as to provide an enhanced deposition rate of the microelectronic layer.

21. (Original) The method of claim 20 wherein the deposition method employs a first pulsed reactant gas, a second pulsed reactant gas and a pulsed purge gas.

22. (Original) The method of claim 20 wherein the deposition method employs a first pulsed reactant gas, a second pulsed reactant gas and a non-pulsed purge gas.

23. (Original) The method of claim 20 wherein the microelectronic layer is selected from the group consisting of conductor layers, semiconductor layers and dielectric layers.

24. (Original) The method of claim 20 wherein the microelectronic layer is a conductor barrier layer.